METHOD OF ATTACHING A DIE TO A SUBSTRATE

BACKGROUND OF THE INVENTION

[0001] The present invention relates to integrated circuits and a method of packaging integrated circuits and, more particularly, to a method of attaching a die to a substrate.

[0002] An integrated circuit (IC) die is a small device formed on a semiconductor wafer, such as a silicon wafer. Such a die is typically cut from the wafer and attached to a substrate or base carrier for interconnect redistribution. Bond pads on the die are then electrically connected to the leads on the carrier via wire bonding. The die and wire bonds are encapsulated with a protective material such that a package is formed. The leads encapsulated in the package are redistributed in a network of conductors within the carrier and end in an array of terminal points outside the package. Depending on the package type, these terminal points may be used as-is, such as in a Thin Small Outline Package (TSOP), or further processed, such as by attaching spherical solder balls for a Ball Grid Array (BGA). The terminal points allow the die to be electrically connected with other circuits, such as on a printed circuit board. IC die can also be attached to other die to form a stacked multichip device.

[0003] Referring now to FIG. 1, an enlarged side view of a conventional TSOP 10 is shown. The TSOP 10 includes an integrated circuit or die 12 attached to a paddle 14 with an adhesive material layer 16. The integrated circuit 12 is electrically connected to pins 18 of a leadframe with wirebonds 20. The circuit 12, paddle 14, and wirebonds 20 are encapsulated, such as with a molded plastic 22.

[0004] The conventional die attach method covers the paddle 14 with an amount of adhesive material 16 that matches the exact die size only. Thus, as shown in FIG. 2, when the integrated circuit 12 is pressed onto the adhesive material 16, the adhesive material 16 only extends beyond the die size by a distance that is equal to about the height of the die or integrated circuit 12.

[0005] FIG. 3 is a top plan view of the integrated circuit 12 attached to the paddle 14 with the adhesive material 16. As can be seen, there is a large portion of the paddle 14 that is not covered by either the integrated circuit 12 or the adhesive material 16.

[0006] Some devices are packaged using an exposed pad (EP) design in order to enhance heat dissipation and improve certain electrical characteristics. In an exposed die attach pad design, the die attach pad is soldered directly onto the PCB. That is, the die is attached directly to a metal paddle, which is directly soldered to the PCB. However, special care must be taken when handling and soldering these EP packages. Such EP packages must be handled in a dry environment prior to soldering and exposure to moisture must be minimized prior to assembly to ensure reliable performance. The coverage of the adhesive material 16 during the die attach process is critical to field operation reliability. Voids and variations in thickness of the adhesive material 16 are undesirable. Further, insufficient coverage of the die attach material 16 makes the device susceptible to reliability failures, due to, for example, delamination. Moisture buildup in the die attach adhesive can also cause delamination. The aforedescribed die attach method only marginally achieves Moisture Sensitive Level Three (MSL-3) at 240°c reflow condition.

[0007] It would be desirable to be able to attach a die to a paddle, substrate or carrier with an adhesive such that the device is less sensitive to moisture and more reliable.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The foregoing summary, as well as the following detailed description of preferred embodiments of the invention, will be better understood when read in conjunction with the appended drawings. For the purpose of illustrating the invention, there is shown in the drawings embodiments that are presently preferred. It should be understood, however, that the invention is not limited to the precise arrangements and instrumentalities shown. In the drawings:

[0009] FIG. 1 is an enlarged cross-sectional view of a conventional thin small outline package;

[0010] FIG. 2 is an enlarged side view of an IC die attached to a carrier in a conventional manner;

[0011] FIG. 3 is an enlarged top plan view the die and carrier of FIG. 2;

[0012] FIG. 4 is an enlarged top plan view of a die attached to a carrier in accordance with a first embodiment of the present invention;

[0013] FIG. 5 is an enlarged side view of the die and carrier of FIG. 4;

[0014] FIG. 6 is an enlarged top plan view of a first pattern of die attach material in accordance with an embodiment of the present invention; and

[0015] FIG. 7 is an enlarged top plan view of a second pattern of die attach material in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0016] The detailed description set forth below in connection with the appended drawings is intended as a description of the presently preferred embodiments of the invention, and is not intended to represent the only forms in which the present invention may be practiced. It is to be understood that the same or equivalent functions may be accomplished by different embodiments that are intended to be encompassed within the spirit and scope of the invention. For simplicity, examples used to illustrate the invention refer to TSOPs. However, the present invention can be applied to other packages and is especially useful for EP type packages in which at least one side of a metal die pad is exposed.

[0017] Certain features in the drawings have been enlarged for ease of illustration and the drawings and the elements thereof are not necessarily in proper proportion. However, those of ordinary skill in the art will readily understand such details. In the drawings, like numerals are used to indicate like elements throughout.

[0018] In order to provide a reliable integrated circuit the present invention is a semiconductor device, comprising a base carrier, an adhesive material layer, and an integrated circuit die. The base carrier has a top side and a bottom side, the top side having a central area and a peripheral area. The central area is for receiving the integrated circuit die. The adhesive material layer is disposed on the top side of the base carrier. The adhesive material layer covers substantially all of the central and peripheral areas of the base carrier top surface. The integrated circuit die is attached to the base carrier with the adhesive material layer at the central area.

[0019] The present invention also provides a novel die attach dispensing pattern that is very effective in enhancing the delamination resistance at the paddle interfaces under JEDEC conditions MSL-1 at 240°c and MSL-2 at 260°c reflow. In accordance with this embodiment, the present invention provides a semiconductor device, comprising a base carrier, an adhesive material layer, and an integrated circuit die. The base carrier has a top side and a bottom side, the top side having a central area for receiving the die and a peripheral area. The adhesive material layer is disposed on the top side of the base carrier. The adhesive material layer is dispensed on the top side of the base carrier in an "X" shaped pattern having two bisecting lines that extend beyond the central area and into the peripheral area of the base carrier top surface. The die is attached to the base carrier with the X-shaped adhesive material layer at the central area.

[0020] The present invention further comprises dispensing die attach material onto a top surface of a paddle such that the die attach material covers substantially the entire top surface of the paddle, regardless of the size of a die to be attached to the paddle. Thus, according to this embodiment, the present invention provides a method of attaching an integrated circuit die to a base carrier comprising the steps of:

[0021] dispensing an adhesive material onto a central area of a top surface of the base carrier, wherein the central area is sized to receive the integrated circuit die and the central area is surrounded by a peripheral area; and

[0022] attaching a bottom surface of the integrated circuit die to the central area on the top surface of the base carrier with the adhesive material, wherein the

adhesive material dispensed onto the top surface of the base carrier extends well into the peripheral area of the base carrier top surface.

[0023] Referring now to FIG. 4, a top plan view of a portion of a semiconductor device 30 in accordance with the present invention is shown. The device 30 includes a base carrier 32 having a top surface (partially visible) and a bottom surface. The top surface has a central area for receiving an integrated circuit die 34 and a peripheral area. As shown in the drawing, the peripheral area surrounds the central area and the die 34. The base carrier 32 is of a type well known to those of ordinary skill in the art. The base carrier 32 may be a lead frame paddle, a printed circuit board, a substrate, *etc.*

[0024] An adhesive material layer 36 is disposed on the top surface of the base carrier 32. The adhesive material layer 36 covers a large part of the central and peripheral areas of the top surface of the base carrier 32. That is, according to the present invention, the device 30 has extended adhesive material coverage. Extended adhesive material coverage means that the adhesive material extends beyond the edges of the die 34 and such extension is greater than or equal to two times the thickness of the die. FIG. 5 is an enlarged side view illustrating how the adhesive material layer 36 extends well beyond the central area (*i.e.*, the perimeter of the die 34) and into the peripheral area.

[0026] The adhesive material 34 is a die attach adhesive preferably of a type well known to those of skill in the art that provides low moisture absorption and thermal dissipation. If a conductive adhesive material is used, it is preferred to provide uniform intermetallic formation. Some example adhesives are solder, epoxy, modified epoxy, and Cyanate Ester blends. The adhesive

material may be filled with particles to increase thermal dispersion properties.

[0027] The integrated circuit die 34 is attached to the base carrier 32 with the adhesive material layer 36 at the central area of the base carrier 32. After the die 34 is attached, the adhesive material is cured, typically at a temperature ranging between 125-175 degrees C. The integrated circuit die 34 may be of a type known to those of skill in the art, such as a circuit formed on and cut from a silicon wafer. The central area of the top surface of the base carrier 32 is sized and shaped to receive the die 34. Typical die sizes may range from 4mm x 4mm to 12mm x 12 mm. The die 34 may have a thickness ranging from about 6 mils to about 21 mils. For example, if the die 34 is 8mm x 8mm x 6 mils, then the central area is 8mm x 8mm and a distance from an edge of the central area to an outer edge of the peripheral area (*i.e.*, the width of the peripheral area) is greater than 12 mils and is usually in a range of about 13 mils to 15 mils.

[0028] As previously discussed, the adhesive material layer 36 extends well beyond the central area and covers substantially all of the top surface of the base carrier 32. In another example, if the die 34 is 8mm x 8mm x 6 mils and the base carrier 32 is 12mm x 12mm, then the adhesive material layer 36 is preferably about 10.4 mm x 10.4 mm.

[0029] In one embodiment of the invention, the base carrier 32 may be a paddle of a leadframe. In such embodiment, bonding pads on the die 34 can be wirebonded to fingers of the leadframe in a well known manner, so that the die 34 is electrically connected to the leadfram fingers. The base carrier or paddle 32, the die 34 and at least a portion of the leadframe fingers may be

encapsulated with a plastic or epoxy resin material, which forms a protective seal. The present invention provides the most benefit to EP type packages because EP packages usually need to maximize the exposed pad regardless of the die size for maximum thermal performance, which creates more cases of a small die on a large die pad. Packages in fully encapsulated form, such as shown in FIG. 1, and packages using an organic substrate, like BGAs, benefit less from the extended adhesive material coverage of the present invention.

[0030] Referring now to FIG. 6, in a preferred embodiment of the invention, the base carrier 32 includes a central area 38 for receiving an integrated circuit die, and a peripheral area. A die attach material 40 is dispensed on a surface of the base carrier 32 in an "X" shaped pattern, with the legs of the "X" extending well beyond the central area 38 and into the corners of the base carrier 32. The "X" shaped pattern includes two bisecting lines that extend beyond the central area 38 and into the peripheral area of the base carrier top surface. An integrated circuit die can then be attached to the central area 38 base carrier 32 with the adhesive material layer. The die attach or adhesive material can be dispensed in controlled amounts on to the base carrier 32 using commercially available equipment.

[0031] Referring now to FIG. 7, in another preferred embodiment of the invention, the base carrier 32 includes a central area 38 for receiving an integrated circuit die, and a peripheral area. A die attach material 42 is dispensed on a surface of the base carrier 32 in a star shaped pattern. As can be seen, the points of the star shaped pattern extend well beyond the central area 38 and into the corners of the base carrier 32. More particularly, the star shaped pattern includes two

bisecting lines that extend beyond the central area 38 and into the corners of the peripheral area of the base carrier top surface. The star shaped pattern can include either one or two additional lines. For example, the pattern may include a first line extending from a middle part of the peripheral area of a first side of the base carrier 32 to a middle part of the peripheral area of a second, opposing side of the base carrier 32 such that the adhesive material layer 42 forms a six pointed star.

[0032] The star shaped pattern can also include a second line extending from a middle part of the peripheral area of a third side of the base carrier 32 to a middle part of the peripheral area of a fourth, opposing side of the base carrier 32 such that the adhesive material layer 42 forms an eight pointed star. An integrated circuit die can then be attached to the central area 38 base carrier 32 with the star shaped adhesive material layer 42.

[0033] In accordance with the present invention, a method of attaching an integrated circuit die to a base carrier includes the steps of dispensing an adhesive material onto the central area of a top surface of the base carrier and then attaching a bottom surface of the integrated circuit die to the central area on the top surface of the base carrier with the adhesive material. As previously discussed, the central area is sized to receive the integrated circuit die and the central area is surrounded by a peripheral area. The adhesive material is dispensed onto the top surface of the base carrier such that it extends well into the peripheral area of the base carrier top surface. The adhesive material is dispensed in a controlled manner and in a predetermined pattern, such as "X" shaped or star shaped.

[0034] The present invention provides a simple and inexpensive way to improve EP package moisture level

performance and does not require any major material changes. The present invention also allows a single lead frame part, with a large die pad, for both large and small size devices, which reduces leadframe inventory variety.

[0035] The description of the preferred embodiments of the present invention have been presented for purposes of illustration and description, but are not intended to be exhaustive or to limit the invention to the forms disclosed. It will be appreciated by those skilled in the art that changes could be made to the embodiments described above without departing from the broad inventive concept thereof. In addition, the die and paddle sizes may vary to accommodate the required package design. It is understood, therefore, that this invention is not limited to the particular embodiments disclosed, but covers modifications within the spirit and scope of the present invention as defined by the appended claims.